

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the Application. The Applicant has amended independent Claims 1, 8 and 15 and has cancelled dependent Claims 2, 9 and 16, without prejudice or disclaimer, and has incorporated these dependent claims into independent Claims 1, 8 and 15, respectively. Support for these amendments can also be found, among other places, in paragraphs [0043-0046] of the Specification. Accordingly, Claims 1, 3-8, 10-15, and 17-20 are currently pending in the Application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 103

The Examiner has rejected Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2002/0085578 A1 to Dell, *et al.* (“Dell”) in view of U.S. patent No. 6,667,983 B1 to Lo, *et al.* (“Lo”) and U.S. Patent No. 6,963,576 to Lee (“Lee”).

Amended Claim 1 is directed to a head blockage avoidance system. The system includes a priority summarizer configured to generate a priority summary of the packets within the m inputs and the n packet FIFOs. *The n packet FIFOs occupy a same hierarchical level. The priority summarizer indicates which of the n packet FIFOs contains or is to receive a highest priority packet from one of the m inputs.* The head avoidance blockage system further comprises a scheduler configured to cause *packets in the n packet FIFOs to be queued for processing based on the priority summary such that packets in a packet FIFO that contains or is to receive said highest priority packets are triggered to be processed before packets in other of said n packet FIFOs.* (Emphasis added.) A “hierarchical level” may be generally defined as wherein a plurality of packet FIFOs or other buffers, such as PKT

FIFO 330 and 332, as being coupled in parallel to a device, such as DEST FIFO 336, as is illustrated in FIG. 3 of the present Application.

Dell is directed to a switching stage that employs crossbar devices. (*See* page 2, paragraph [0013]). In Dell, the “switch fabric of the present invention is a cell-switching engine handling *fixed-sized* switching cells.” (*See* page 6, paragraph [0090]). Dell uses one or more crossbars to achieve scalability in self-routing of cells. (*See* page 2, paragraph [0012]).

Lo is directed to a scalable arbiter for arbitrating between multiple FIFO entry points of a network interface card. (*See* Abstract.) Lee is directed toward an arbitration scheme that is used for scheduling connections between input ports and output ports.

The Examiner admits, and the Applicant agrees, that Dell does not disclose a priority summarizer configured to generate a priority summary of the packets within inputs and a scheduler configured to cause one of the packet FIFOs to be queued for processing based on the priority summary. (*See* Examiner's Action, page 4.)

However, the Examiner cites Lo for disclosing:

a scheduler configured to cause one of the packet FIFOs to be queued for processing based on an order indicated by the priority summary (See column 10 line 42 to column 11 line 44 and Figures 8A-B of Lo et al. for reference to arbiter circuit 420, which is a scheduler, that selects a FIFO to be processed for packet transmission based on the priority information of packets stored in the FIFOs of circuit 405). (*See* Examiner's Action, page 5.)

In Lo, Column 11, lines 14-33:

As shown in FIG. 8B [reproduced below for the Examiner's convenience], scaleable arbiter circuit 420 is a multi-staged circuit having one stage for each separate transmission priority and contains exemplary stages 430a-430d. The first stage 430a is triggered based on a predetermined time interval that first allows an isochronous data packet to be transmitted through its input A. After transmission, input B can be selected

which gives a downstream priority stage an opportunity to transmit. *Based on the toggle activity of each sequential circuit, and assuming all stages always have packets to transmit, in one embodiment, 1/2 bandwidth is given to the isochronous transmissions, 1/4 to priority 1 packets, 1/8 to priority 2 packets and so forth.* However, on any stage's transmission turn, if it does not have a data packet of its own priority for transmission, then it automatically selects its input "B" to allow a downstream priority an opportunity to transmit a packet. Once a stage transmits some data of its associated transmission priority, it automatically toggles its sequential circuit for its next transmission turn. (Emphasis added.)

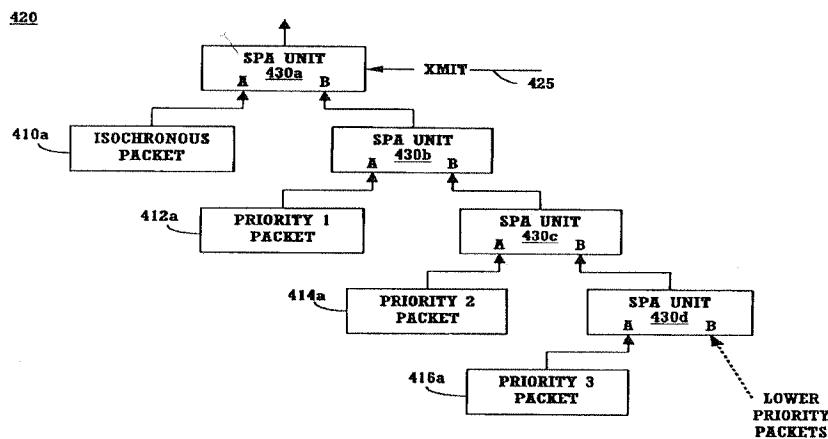


FIGURE 8B

The scalable arbiter circuit 420 is unlike the scheduler of amended Claim 1. In Claim 1, if an n packet FIFO contains or is to receive the highest priority packet, packets in that packet FIFO are triggered to be processed before packets in the other packet FIFOs.

For example, in one embodiment discussed in the present Application (paragraphs [0045-0046]):

[In one embodiment], the scheduler 360 may determine from the priority summary which of the first and second packet FIFOs 330, 332 is to be queued to transfer one of the packets within the first and second FIFOs 330, 332 toward the destination FIFO 336 for transmission to the first output. The priority summary may indicate that the first FIFO 330 contains a packet having a low priority and the second FIFO 332 contains a packet having a medium priority. The priority summary may also indicate that the first source FIFO 310 contains a packet having a high priority and that the second source FIFO 320 contains a packet having a medium priority. ... In order to prevent head of line blockage of the packet having a high

priority in the first source FIFO 310 by the packet having a low priority in the first packet FIFO 330, the scheduler 360 would queue the first packet FIFO 330 to be processed first. This would allow the packet having the low priority in the first packet FIFO 330 to be transferred to the destination FIFO 336. Then, the packet having a high priority would be transmitted toward the first packet FIFO 330 and the first packet FIFO 330 would be processed next. Thus, the head of line blockage is avoided.

Lo's scalable arbiter circuit 420 is hierarchical and thus differs significantly from the scheduler of amended Claim 1. For example, in one of Lo's embodiments (based on the toggle activity of each sequential circuit and assuming all stages always have packets to transmit), 1/2 bandwidth is given to the isochronous transmissions, 1/4 to priority 1 packets, 1/8 to priority 2 packets and so forth. As is discussed and further illustrated in FIGURE 8B of Lo, above, stages 430-430d of Lo occupy differing "hierarchical levels," and the contents of the stages received bandwidth in proportion to their position within the hierarchy of the scaleable arbiter circuit 420. However, in amended Claim 1, if an n packet FIFO contains or is to receive the highest priority packet, packets in that packet FIFO are triggered to be processed before packets in the other packet FIFOs.

In view of the foregoing remarks, the cited references do not support of the Examiner's rejection of independent Claim 1, nor for similar reasons the rejection of independent Claim 8 and Claim 15, nor their dependent claims, when considered as a whole. Therefore, Claims 3-8, 10-15, and 17-20 are nonobvious over the cited references under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection of Claims 1, 3-8, 10-15, and 17-20 and allow issuance thereof.

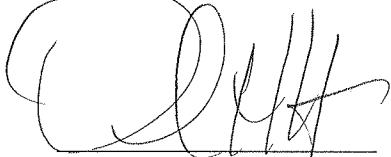
II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this Application to be in condition for allowance and therefore earnestly solicit s a Notice of Allowance for Claims 1, 3-8, 10-15, and 17-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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Dated: May 21, 2007

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